



PTO/SB/08 (2-92)

Sheet 1 of 3

Form PTO-1449

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

(Use several sheets if necessary)

Docket Number 306812002201

Application Number 10/650,465

Applicant

Brian D. JOHNSON et al.

Filing Date August 27, 2003

Group Art Unit Not Yet Assigned

Mailing Date November 20, 2003

## U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
<i>je</i>	1.	10/25/2001	2001/0033188	Aung et al.			
	2.	09/26/1989	4,870,302	Freeman			
	3.	10/03/1989	4,871,930	Wong et al.			
	4.	06/09/1992	5,121,006	Pedersen			
	5.	08/31/1993	5,241,224	Pedersen et al.			
	6.	09/07/1993	5,243,238	Kean			
	7.	11/09/1993	5,260,611	Cliff, et al.			
	8.	10/25/1994	5,359,536	Agrawal et al.			
	9.	10/03/1995	5,455,525	Ho, et al.			
	10.	01/16/1996	5,485,103	Pedersen, et al.			
	11.	07/16/1996	5,537,057	Leong, et al.			
	12.	07/30/1996	5,541,530	Cliff, et al.			
	13.	08/27/1996	5,550,782	Cliff et al.			
	14.	09/17/1996	5,557,217	Pedersen			
	15.	12/03/1996	5,581,199	Pierce, et al.			
	16.	01/07/1997	5,592,106	Leong, et al.			
	17.	10/28/1997	5,682,107	Tavana, et al.			
	18.	11/18/1997	5,689,195	Cliff, et al.			
	19.	12/23/1997	5,701,091	Kean			
	20.	01/06/1998	5,705,939	McClintock, et al.			
	21.	06/02/1998	5,760,604	Pierce et al.			
	22.	12/08/1998	5,847,579	Trimberger			
	23.	03/09/1999	5,880,598	Duong			
	24.	05/11/1999	5,903,165	Jones et al.			
<i>je</i>	25.	05/25/1999	5,907,248	Bauer, et al.			
<i>je</i>	26.	06/01/1999	5,909,126	Cliff, et al.			

EXAMINER:

*James K. Chu*

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*5-6-04*

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JL	27.	06/22/1999	5,914,616	Young, et al.			
	28.	08/24/1999	5,942,913	Young, et al.			
	29.	11/02/1999	5,977,793	Reddy et al.			
	30.	12/14/1999	6,002,268	Sasaki et al.			
	31.	07/04/2000	6,084,429	Trimberger			
	32.	08/22/2000	6,107,824	Reddy, et al.			
	33.	03/20/2001	6,204,690	Young, et al.			
	34.	04/17/2001	6,218,859	Pedersen			
	35.	08/21/2001	6,278,291	McClintock, et al.			
	36.	09/11/2001	6,289,412	Yuan et al.			
	37.	09/18/2001	6,292,018	Kean			
	38.	10/09/2001	6,300,794	Reddy, et al.			
	39.	11/19/2002	6,484,291	Amiya et al.			
JL	40.	08/12/2003	6,605,962	Lee et al.			

## FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO

## OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title
JL	41.	Altera Corporation (June 1996). "Max 7000: Programmable logic device family" Data Book, A-DB-0696-01, version 4, pp. 193-261.
JL	42.	Altera Corporation (October 2001). Excalibur "Description of the The Floor plan", pp. 1-1 through 1-10.
JL	43.	Betz, V. et al., eds. (1999) "Background and Previous Work," Chapter 2 In <u>Architecture and CAD for Deep-Submicron FPGAs</u> , Kluwer Academic, Boston pp. 12-18.
JL	44.	Betz, V. et al., eds. (1999). "Routing Tools and Routing Architecture Generation," Chapter 4 In <u>Architecture and CAD for Deep-Submicron FPGAs</u> , Kluwer Academic, Boston, pp. 63-95.
JL	45.	Betz, V. et al., eds. (1999). "Detailed Routing Architecture," Chapter 7 In <u>Architecture and CAD for Deep-Submicron FPGAs</u> , Kluwer Academic, Boston, pp.151-190.

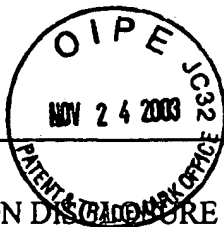
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*James A. Cho*

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|-----------|-----|---|
| <i>jk</i> | 46. | Betz, V. et al., eds. (1999). "Global Routing Architecture," Chapter 5 In <u>Architecture and CAD for Deep-Submicron FPGAs</u> , Kluwer Academic, Boston, pp. 105-126.  |
| <i>jk</i> | 47. | Xilinx. (November 2000). "Programmable Logic: News and Views, a monthly report on developments in the PLD/FPGA industry" <i>Electronic Trend Publications, Inc.</i> , IX(11):14-15. (Includes Table of Contents). |
| <i>jk</i> | 48. | Xilinx. (October 2000) "Putting It All the Together. The Vitrex-II Series Platform FPGA: World fastest logic and routing" Xilinx brochure, p. 83.   |

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